FIG. 1

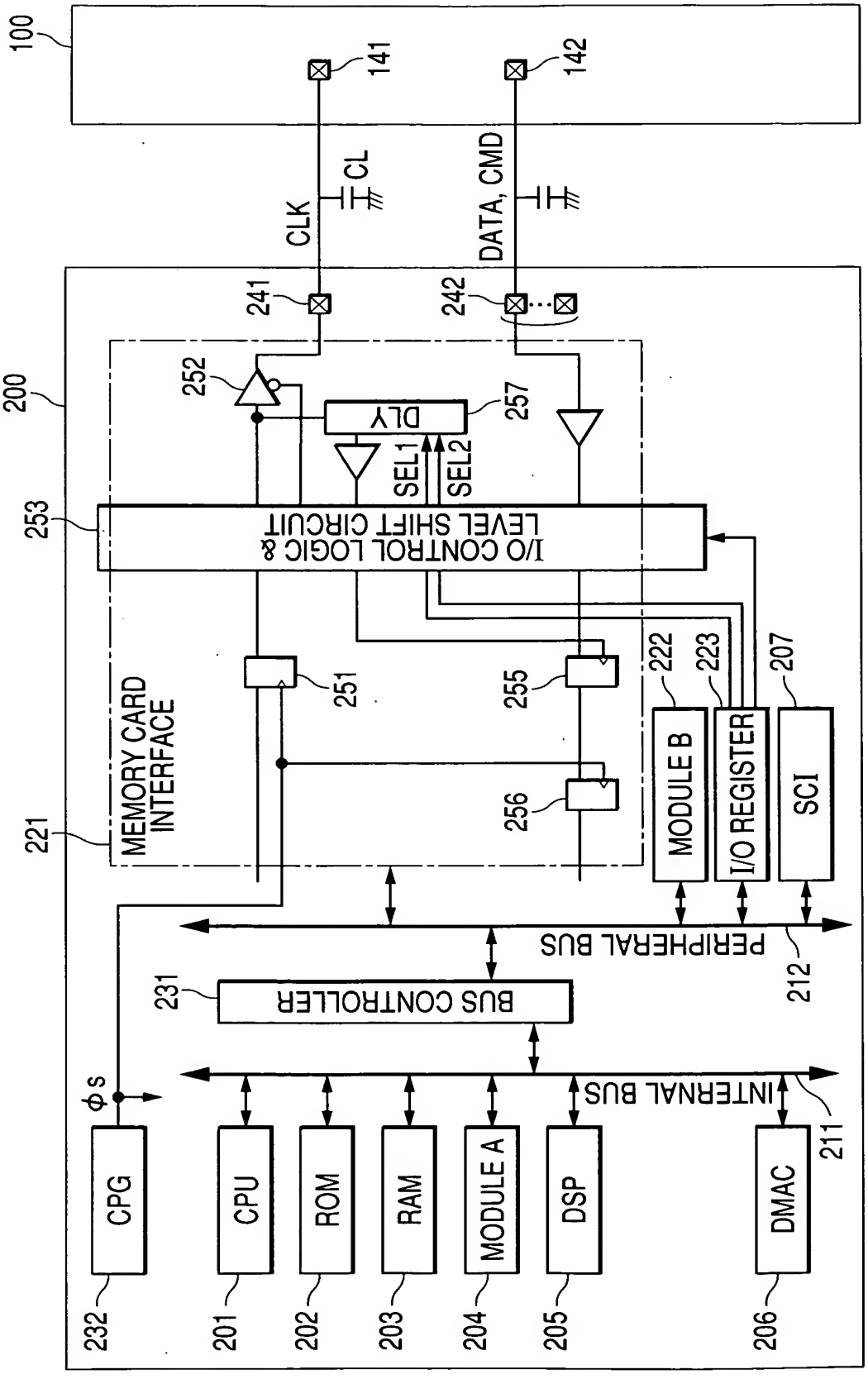

100
141
142
CLK
CL
DATA, CMD
241
242
200
252
DLY
257
SEL1
SEL2
253
I/O CONTROL LOGIC & LEVEL SHIFT CIRCUIT
251
255
256
221
MEMORY CARD INTERFACE
222
223
207
MODULE B
I/O REGISTER
SCI
PERIPHERAL BUS
212
231
BUS CONTROLLER
INTERNAL BUS
211
φs
CPG
CPU
ROM
RAM
MODULE A
DSP
DMAC
232
201
202
203
204
205
206

FIG. 2

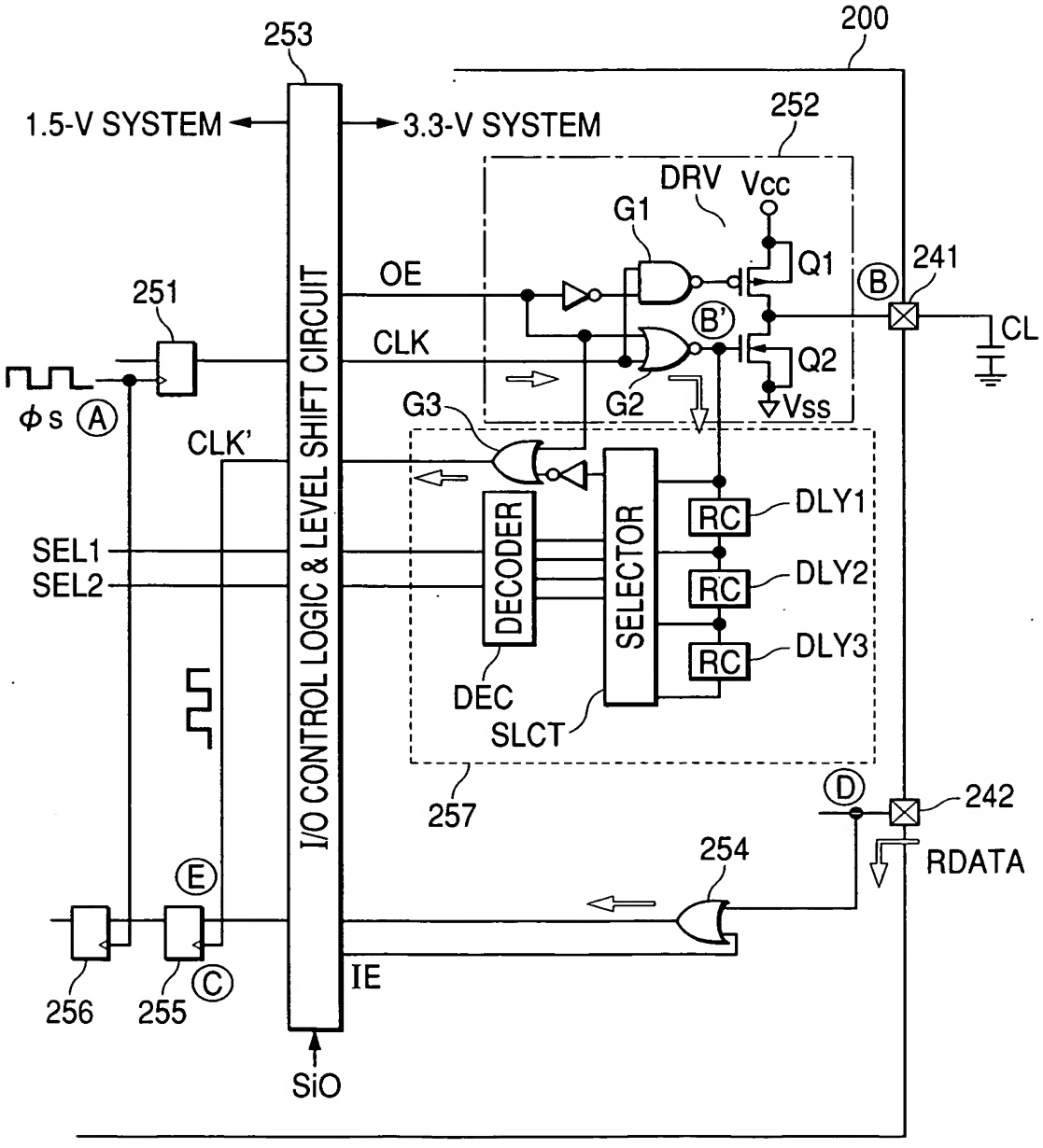

253
200
1.5-V SYSTEM
3.3-V SYSTEM
252
DRV
Vcc
G1
Q1
241
OE
251
B
B'
CL
CLK
Q2
Vss
G2
G3
CLK'
ϕs
A
SEL1
SEL2
DECODER
SELECTOR
RC
DLY1
DLY2
DLY3
DEC
SLCT
257
D
242
RDATA
254
E
C
256
255
IE
I/O CONTROL LOGIC & LEVEL SHIFT CIRCUIT
SiO

FIG. 3(A)

FIG. 3(B)

FIG. 3(C)

FIG. 3(D)

FIG. 3(E)

FIG. 3(F)

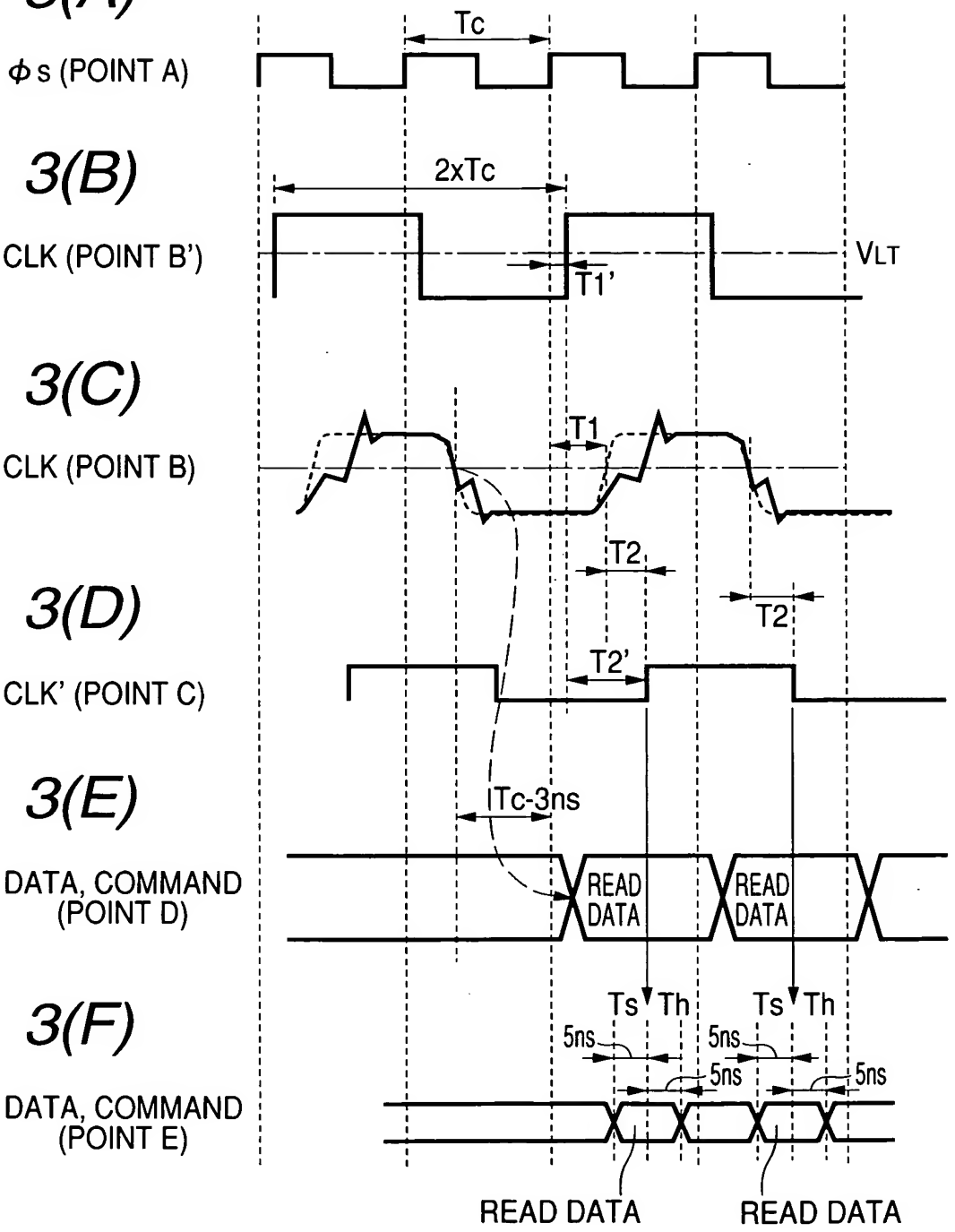


FIG. 4(A)

FIG. 4(B)

FIG. 4(C)

FIG. 4(D)

FIG. 4(E)

FIG. 4(F)

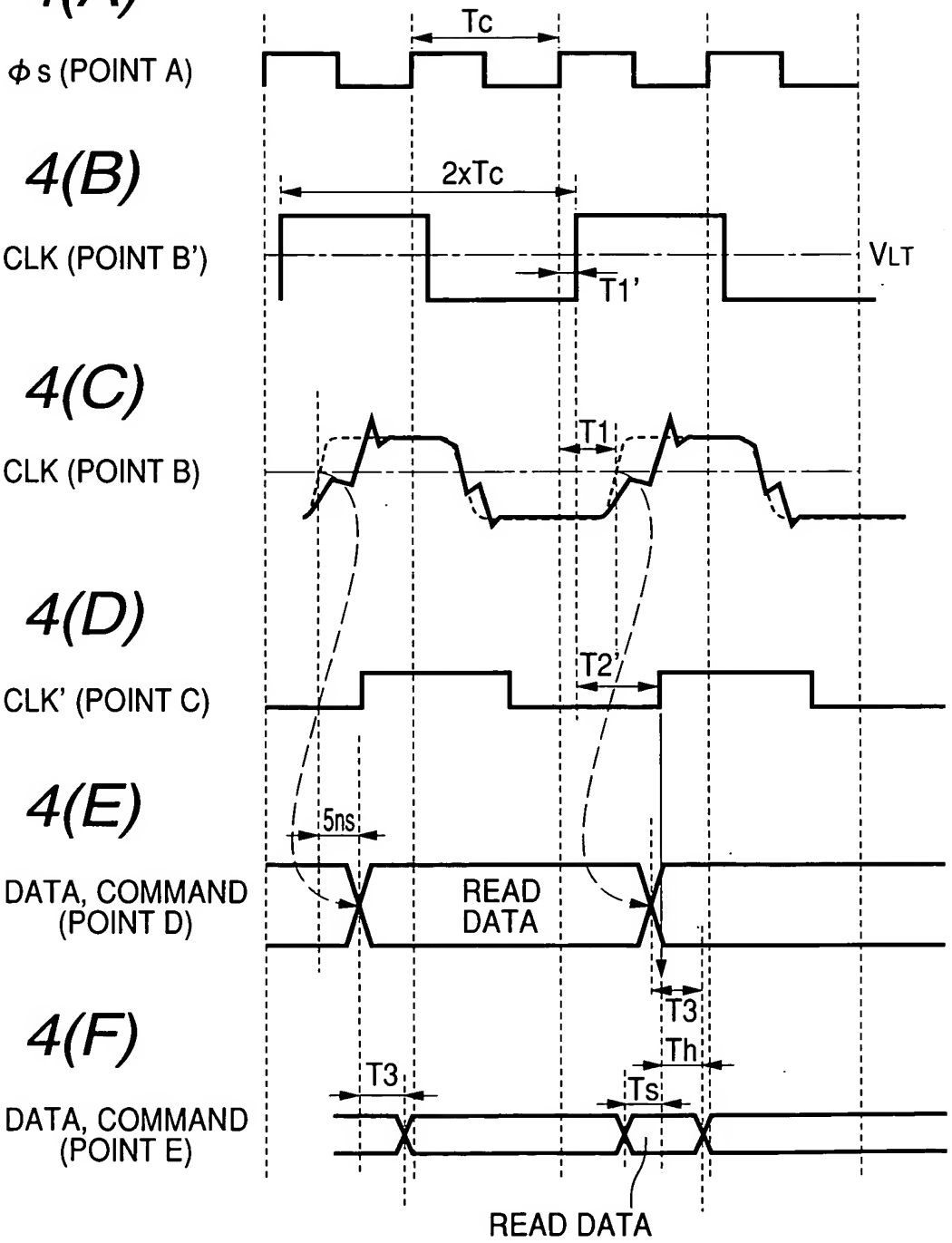


FIG. 5

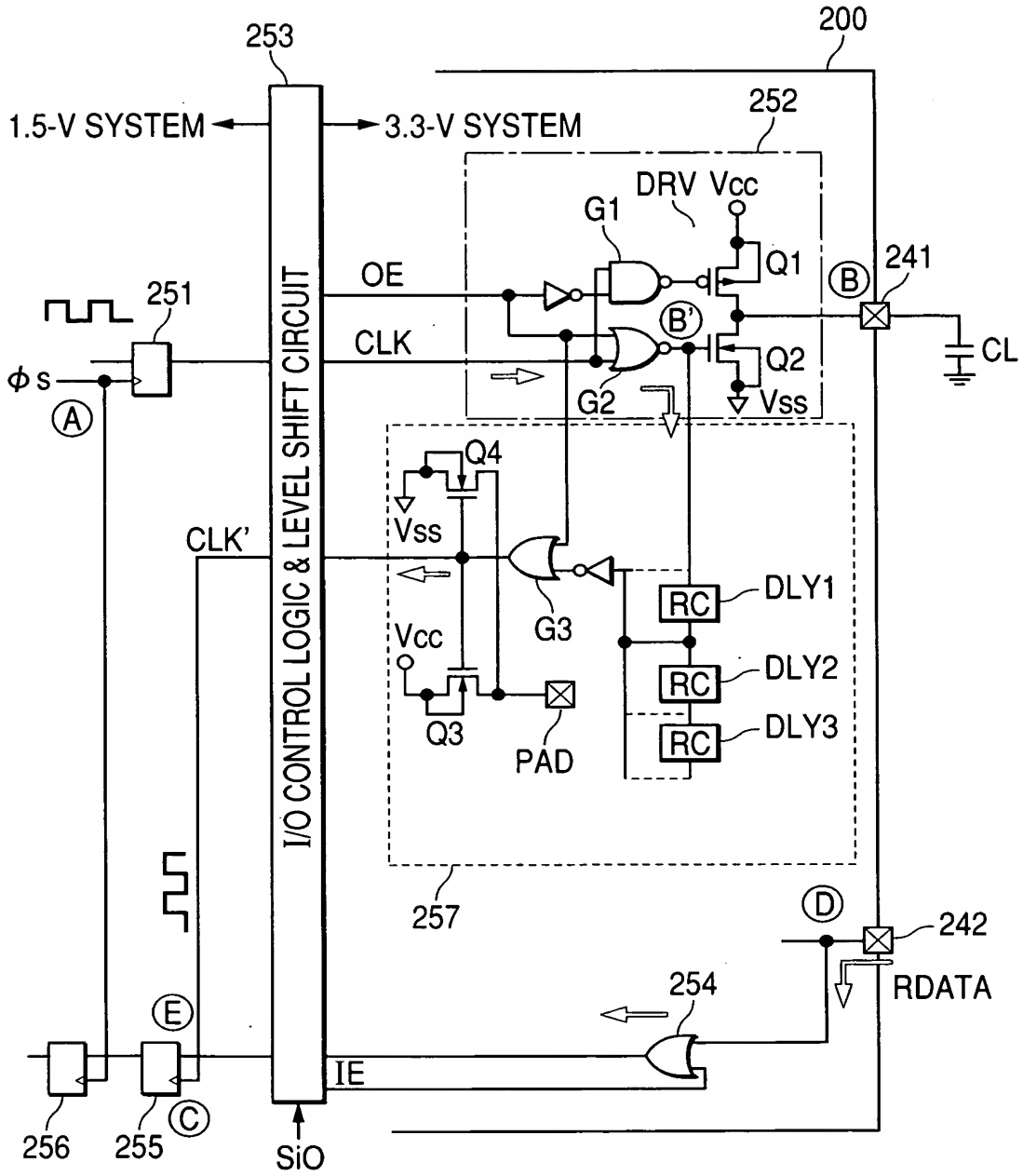

200
253
252
1.5-V SYSTEM
3.3-V SYSTEM
DRV Vcc
G1
Q1
241
B
OE
251
B'
CLK
Q2
CL
φs
G2
Vss
A
Q4
Vss
CLK'
I/O CONTROL LOGIC & LEVEL SHIFT CIRCUIT
RC
DLY1
G3
Vcc
RC
DLY2
Q3
PAD
RC
DLY3
257
D
242
RDATA
254
E
IE
256
255
C
SiO

FIG. 6

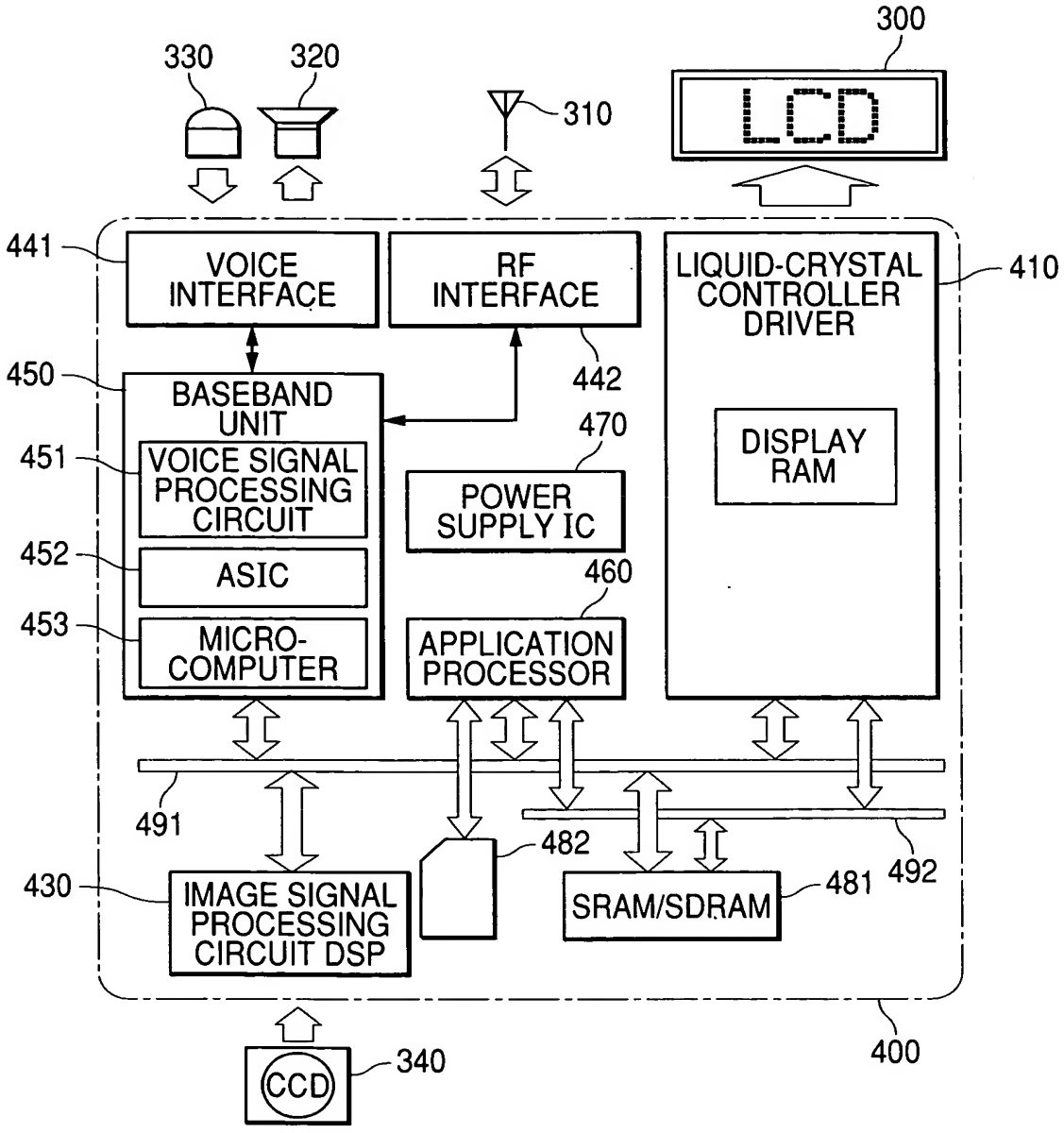

300
LCD
330
320
310
441
VOICE INTERFACE
RF INTERFACE
LIQUID-CRYSTAL CONTROLLER DRIVER
410
442
450
BASEBAND UNIT
470
DISPLAY RAM
451
VOICE SIGNAL PROCESSING CIRCUIT
POWER SUPPLY IC
452
ASIC
460
453
MICRO-COMPUTER
APPLICATION PROCESSOR
491
482
492
430
IMAGE SIGNAL PROCESSING CIRCUIT DSP
SRAM/SDRAM
481
CCD
340
400

FIG. 7

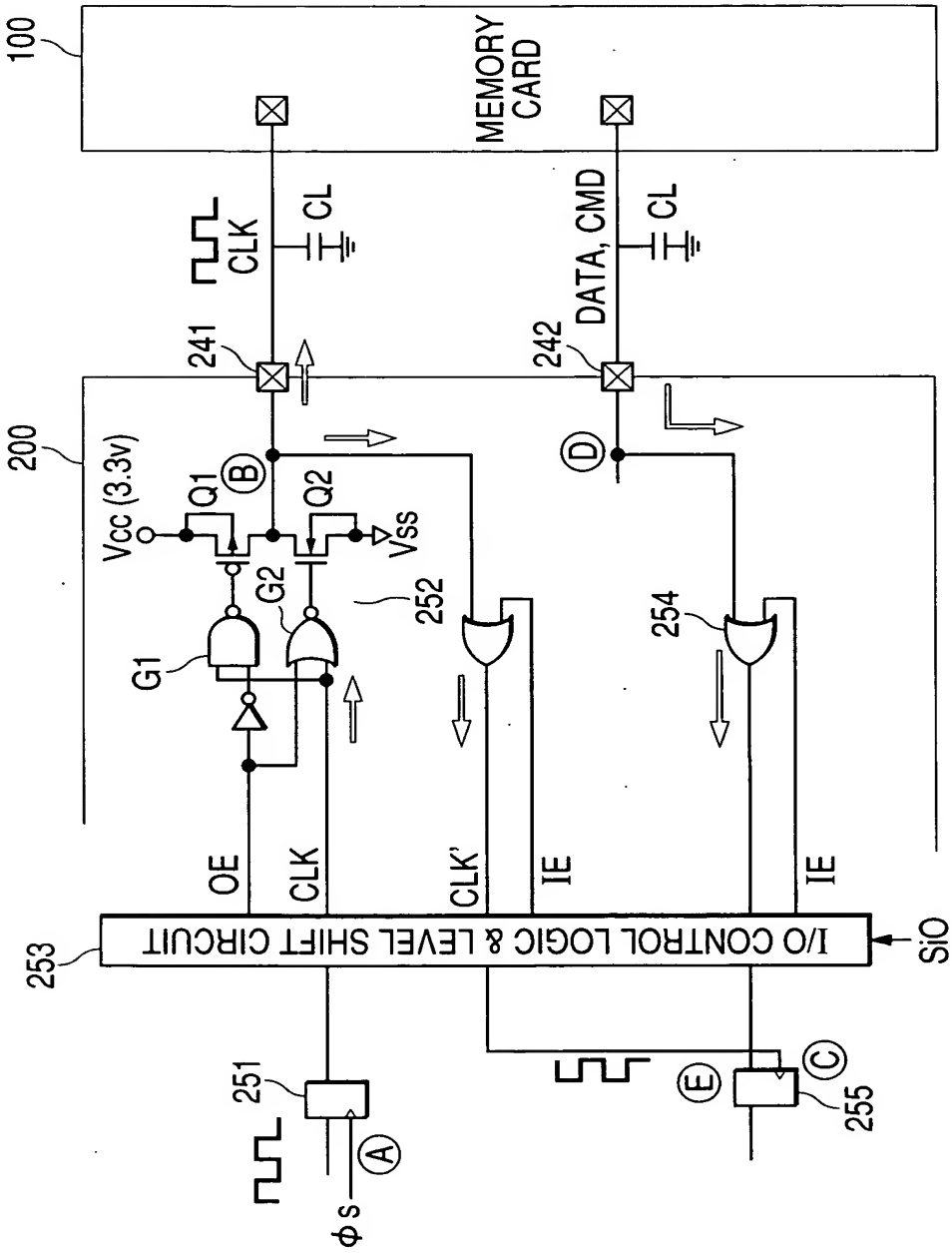

100
MEMORY CARD
CLK
CL
DATA, CMD
CL
241
242
200
Vcc (3.3v)
Q1
B
Q2
Vss
D
G2
252
254
G1
OE
CLK
CLK'
IE
IE
253
I/O CONTROL LOGIC & LEVEL SHIFT CIRCUIT
SIO
251
A
φs
E
C
255

FIG. 8(A)

φs (POINT A)

FIG. 8(B)

CLK (POINT B)

FIG. 8(C)

CLK (POINT C)

FIG. 8(D)

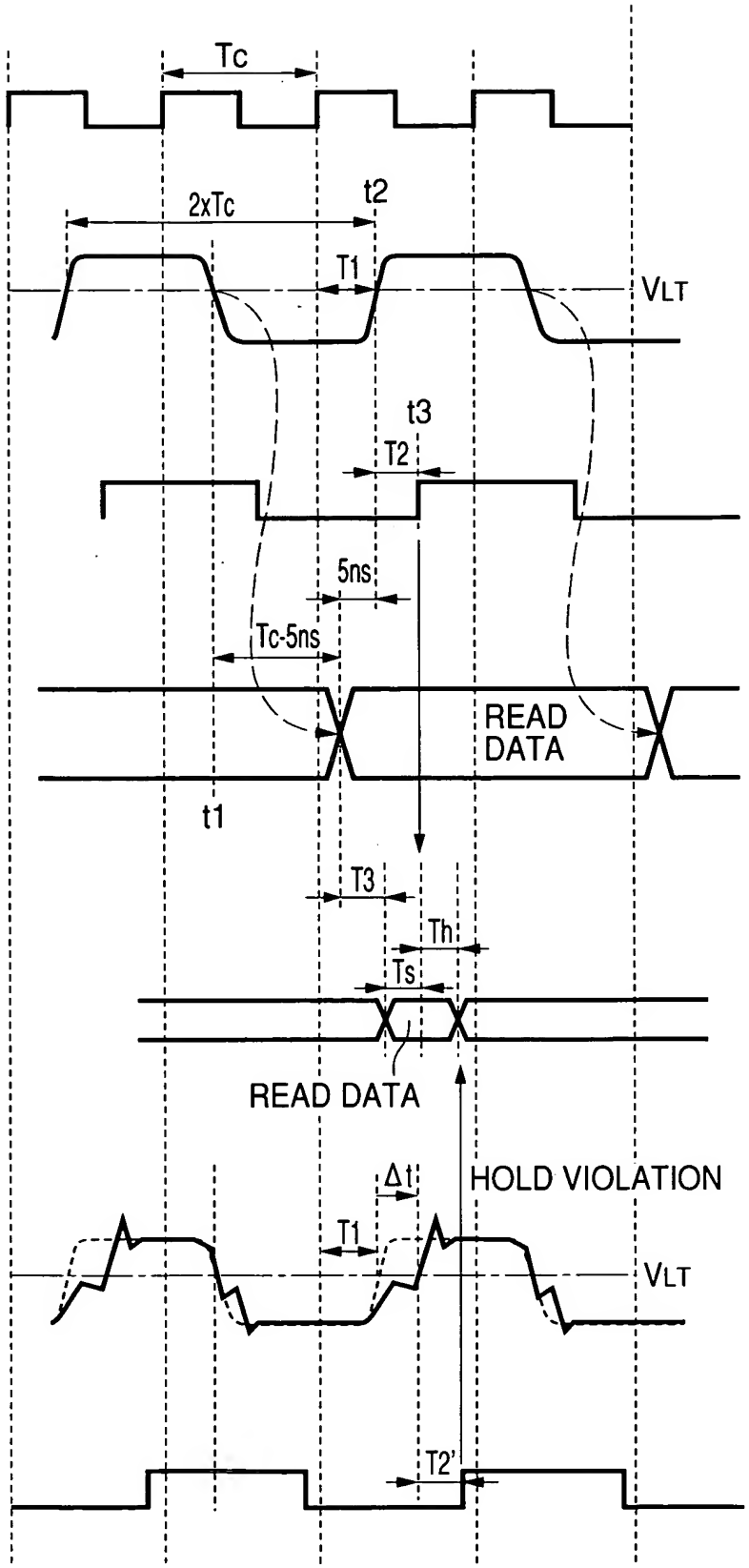
DATA, COMMAND (POINT D)

FIG. 8(E)

DATA, COMMAND (POINT E)

FIG. 8(F)

CLK (POINT B)

FIG. 8(G)

CLK' (POINT C)